REMARKS

Claims 1-28 are pending. Claims 1, 3-17, 19-24, and 26-28 are rejected. Claims 2, 18, and 25 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten to incorporate base and intervening claim limitations. The allowability of claims 2, 18, and 25 is gratefully acknowledged.

Independent claims 1, 17, and 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Inaba (4,396,987). Inaba does not mention any programmable chip or programmable chip system. The Examiner argues that Inaba describes a printed circuit board in a "machine tool and robot control apparatus" and that making integral onto a programmable chip does not provide a patentable distinction. Applicants respectfully submit that claims 1, 17, and 24 are not merely making integral what was described in Inaba.

Inaba describes a robot command system. "The robot command data delivered by the robot control device RC is stored in the data memory DMN in a manner explained hereinunder. Namely, the robot command data, which is delivered by the robot control device RC in a bit-serial manner bit by bit is written in series in the buffer register BFR by the controlling operation of the read/write control circuit RWC. On the other hand, the processing unit MPUN periodically produces the address of the reading gate AGR, so that the reading gate is opened when the decoder ADEC decodes the address. In consequence, the 1 byte robot command data stored in the buffer register BFR is delivered to the data bus DBUS and is temporarily stored in the working memory WMN. Then, the robot command data is written in the date memory DMN by the control of the processing unit MPUN. This operation is repeated to successively store the robot command data in the data memory DMN." (Column 3, lines 33-50)

The independent claims recite a streaming output peripheral on the programmable chip configured to generate clock cycle accurate output signals. Inaba merely describes a control device on a board without mentioning on programmable chip or any clock cycles or clock cycle accurate output signals. In fact, it appears that Inaba may have no clock whatsoever, unlike a programmable chip such as an FPGA or CPLD. Inaba does read information from a memory and does control operation by sending in a "bit-serial manner bit by bit" data.

However, it is not clear from Inaba how Inaba would synchronize the bit by bit data with a system clock or some other clock. In fact, it is not clear that Inaba is concerned with clock cycle accurate output signals at all and the robot arm control bits appear to be written in a manner that does not require clock cycle accuracy. The Examiner may argue that it would be obvious to have clock cycle accurate waveforms. The Applicants respectfully disagree. As noted in the specification, "system processors and microcontrollers can also be used to generate relatively generalized waveforms. However, microcontrollers can not generate clock cycle accurate waveforms. In one example, an interrupt or a processor stall can prevent a processor from outputting a signal at precisely the right clock cycle. Although processors can effectively generate generalized waveforms that are not clock cycle accurate, processors have difficulty generating time precise waveforms." (page 6, liens 18-23)

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable. Applicants believe that all pending claims are allowable for at least the reasons noted above. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned at the number set out below.

Respectfully submitted,
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